Industry Semiconductor Test Solutions for Academic Laboratory Programs

by

Joanna Gatlin, B.S.E.E.

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Approved

Dr. Richard Gale
Chair of Committee

Dr. Stephen Bayne

Dr. Timothy Dallas

Mark Sheridan
Dean of the Graduate School

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ABSTRACT

Industrial sized test systems do not always have flexible applications in university laboratories, although they do provide invaluable learning opportunities for students looking to work in the field of semiconductor test. This project focused on tailoring a recently donated National Instruments Semiconductor Test System (STS) for the Program for Semiconductor Product Engineering Lab at Texas Tech, including the selection of new, cost-effective equipment to extend the flexibility of the system and the design and test of a new device interface board. This board allows students to test a wide variety of devices for the classroom and general research projects.

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LIST OF ABBREVIATIONS

ATE – Automated Test Equipment

ADC – Analog to Digital Converter

DAC – Digital to Analog Converter

DUT – Device Under Test

DIO – Digital Input/Output (I/O)

HSDIO – High Speed Digital Input/Output

NI – National Instruments

PCI – Peripheral Component Interconnect

PPMU – Precision Power Measurement Unit

PSPE – Program for Semiconductor Product Engineering (at Texas Tech)

PXI – PCI eXtensions for Instrumentation (also used in National Instrument's part names)

SMU – Source Measurement Unit

STS – Semiconductor Test System (formerly known as the "Savage Tester")

TI – Texas Instruments

VI – Virtual Instrument (programs within NI's LabVIEW software)

CHAPTER 1

INTRODUCTION

1.1 Motivation

As semiconductor devices become smaller, faster, and more sophisticated pieces of equipment, their corresponding test environment is also expected to evolve along the same terms. Test equipment is expected to condense to less space, reduce test time, and become smarter as to identify problems early and increase product yield. Entire careers can be devoted to maximizing test efficiency and designing flexible manufacturing floor equipment.

Most recently, National Instruments donated a first generation Semiconductor Test System (STS) – the company's answer for catering to industrial semiconductor test solutions [1] – to the Program for Semiconductor Product Engineering (PSPE) lab at Texas Tech University. This equipment opens the door to many students interested in test as a career, as most semiconductor production lines now use Automated Test Environments (ATEs) like the STS. Use of the PSPE lab, and equipment like the STS tester, is not only limited to participating students – several classes within the department allow access to the lab.

While the STS is customizable to a wide variety of applications in industry (it has the option of adding 1-4 fully stocked modular instrumentation chassis [1]), there had been few disclosed developments into broad-spectrum semiconductor test use at the time the STS had been donated. Traditionally, companies that require advanced testing equipment either buy an entire system and device interface board (DIB), customized to their specific semiconductor's needs, or build their own [2]. The STS is aimed at providing a PXI platform's added flexibility (as instrumentation is easily interchangeable), at a potentially lower cost for developer's [1].

Academic research laboratories like PSPE, however, do not have the income to justify highly specialized equipment for the many devices students wish to test, despite the already lower cost/flexibility of the STS and subsequent PXI systems. An even broader solution was necessary in order to encourage student use of the STS.

1.2 Current Equipment

Prior to the arrival of the STS (formerly nicknamed the "Savage"), the PSPE lab already included a single PXI chassis with several Source Measurement Units (SMUs), Digital I/Os (DIOs), and a switch matrix to access the High Speed Digital I/O (HSDIO) output. A "load board" had been designed by several undergraduates to simply output the connectors from each modular instrument to vertical connectors on the board accessible with standard 22-gauge wire. The lab also includes a Texas Instruments' Very Low Cost Tester (VLCT), a temperature chamber, and several Keithley precision SMUs and Ammeters.

Students quite frequently had trouble with the PXI/load board setup, as documentation was not adequately controlled and breadboard setup was sometimes difficult to debug, so more often than not, it was observed that they chose to work with the several pieces of bench-top equipment also located within the lab. Furthermore, exposed cables to and from the PXI instrumentation were prone to tampering when the equipment was not functioning as expected. If setup can be made simpler, time on equipment could be reduced, and backup on equipment could potentially be lessened.

The new STS platform had already solved many of these issues within academia – such as tampering (chassis are now held underneath a clamshell, and cables are not visible to students [1]) and breadboard setup (a single output cable connects to standard DSUB connectors that can be designed onto simple breakout PCBs) – but several major problems still existed. This project aimed at tailoring a new system to meet the needs of present and future test research to be conducted within the lab.

CHAPTER 2

ADDRESSING CURRENT USAGE OF PSPE EQUIPMENT

2.1 Projects in PSPE

A large number of projects within Texas Tech's PSPE Lab center around two courses – ECE 5365 (Parametric Device Testing) and ECE 5366 (Testing of Digital Systems). Most recently, a Topics in Electrical Engineering class has a section called Advanced Modular IC Testing that is devoted to projects on the donated STS. At the conclusion of these courses, students are typically asked to present a project that focuses on testing a chosen device and, in the two earlier mentioned sections, include a test plan of what tests are to be performed and what equipment will be used. This device testing can vary from simple logic gates to complex Analog to Digital Converters (ADC) or Digital to Analog Converters (DAC). Most graduate students are asked to complete a test project that has more difficulty than a logic gate.

What a full scope of tests entails can vary between device, manufacturer, and test engineer [2], so it is left up to the student to choose what test runs would be most appropriate to complete. Some traditional tests that were observed in the Fall 2014 semester included:

- Continuity – the testing of the Device Under Test's (DUT's) ESD protection diodes on certain device pins. This test typically involves driving power pins to zero volts and forcing current on I/O pins to measure the voltage drop across the diodes. [3]
- Power Consumption – the testing of the device's total power consumption. Can use both voltage and current measurements on the DUT's supply pins [4].
- Quiescent Current (I_{DDQ}) – the testing of the device's current draw in different modes of operation to identify manufacturing faults between states [4].
- Functionality – the testing of overall functionality of the device.

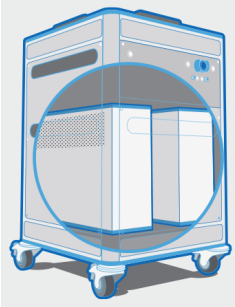
- Leakage (I_{IH}/I_{IL}) – The testing of high-impedance input pins to test for physical defects (shorts) by driving pins to input high or low threshold voltages, and measuring the resulting current for each [3].
- Voltage Output High/Low (V_{OH}/V_{OL}) – the testing of the threshold output voltage. [3] Includes minimum voltage to be considered logic high (V_{OH}) and maximum voltage to be considered logic low (V_{OL})
- High/Low Level Input Voltage (V_{IH}/V_{IL}) – the testing of the logic voltage levels expected by inputs the device, whether they be understood logic high or logic low [3].

Students are also encouraged to test multiple devices in order to obtain a standard distribution of values and run statistical analysis on the results. From the tests listed above, it can be assumed that a generic scope of tests would include instrumentation built to handle current and voltage measurements on almost all device pins. For devices that do not require programming to set inputs and outputs – such as logic gates or JK flip-flops – testing is made easier because no timed device communication, like clocks and serial data, is required for test setup.

2.2 Analyzing Donated Equipment and Reproduction Issues

National Instruments not only donated the T4 STS, but also a PXI-1078 chassis stocked with a PXIe-4140 SMU, a PXIe-6556 HSDIO, and a PXI-2567 Relay Driver. A dual load board (or dual Device Interface Board) setup sits atop the clamshell and hosts connections for all equipment. It is the lab's understanding that this setup was part of a Malaysian company's initial manufacturing run on one of the first STS models. Below is an illustration of the system's structure.

(a)



(b)

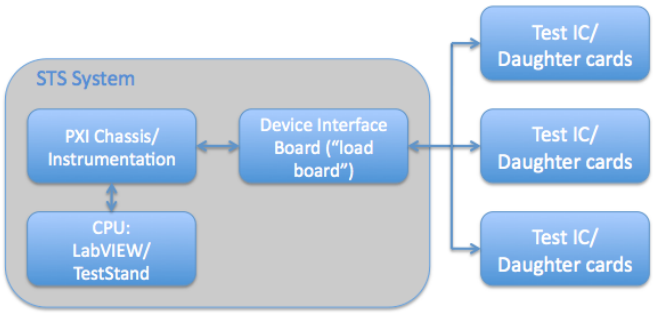


Figure 1: STS Tester: (a) inside T2 System and (b) overall block diagram

In most test cases, a PXIe-4140 4-Channel SMU and a PXIe-6556 HSDIO have all of the capabilities necessary to run a full set of tests. Most setups require the SMU to power the device via V_{CC}, GND, and, occasionally, analog pins; and the HSDIO to handle tests on serial communication and digital logic pins, as illustrated below by one of National Instruments' testing tutorials.

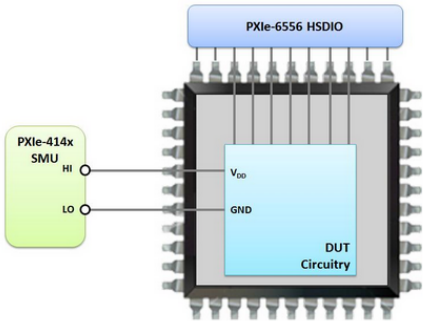


Figure 2: Continuity Test Suggested Setup [4]

HSDIO instruments that come equipped with Precision Power Measurement Units (PPMUs) can also be used in place of an SMU if the current and voltage specifications of

the test fit with that of the HSDIO. [5] Table 1 is a very brief comparison of the SMU specifications versus that of the HSDIO's PPMU.

Table 1: Comparison of HSDIO and SMU Capabilities [5][6]

	PXIe-6556 (HSDIO)	PXIe-4140 (SMU)
Voltage Range	-2 V to 6 V (default)	±10 V
Voltage Resolution	228 µV	100µV
Current Range	±35 mA	±100 mA
Current Resolution	7.3 µA (max)	1 µA (max)

In cases where higher precision and larger current is necessary, the PXIe-4140 is an ideal choice. When students are programming their first testing projects, however, use of HSDIO on logic and power pins is usually sufficient, especially in the lower current ranges where current resolution is magnitudes better [5]. For example, the SN74HC00 (TI's Quad 2-Input Positive NAND Gate) is a popular, inexpensive device used in PSPE to teach basic testing principles. With a 2 V to 6 V input supply and a maximum I_{CC} of 20 µA, [7] exclusive use of the HSDIO will not dramatically affect test results when students are only concerned with verifying what is listed on the datasheet.

2.2.1 Joy Signal Connector and Cable

At first inspection of the given equipment, the only output from the top of the STS load board comes through a Joy Signal 100-pin connector. All PXI equipment connects through the "bottom" of the PCB, and all lines terminate through the Joy Signal connector interface on the top. A custom cable breaks this 100-pin connector into four 25-pin DSUB connectors, allowing for up to four outlets for multisite testing. The term "multisite," in this sense, not only means that testing can be performed on different PCBs – it also indicates that, as long as the sites are of identical pin out, code written can be performed in parallel in certain instances, thus reducing test time. Part of the donation of the STS included a multisite add-on to National Instrument's TestStand software called TestStand Semiconductor Module, used in many of the programming demos created as a result of this project.

The cable does breakout into four separate sites, but this particular load board does not include multisite capabilities, thus limiting current use of the software. Upon further inspection of the board schematic, over 75% of the connections on the Joy Signal connector are either grounded (for shielding) or not connected to any instrumentation through the STS. A section of the schematic, shown below, indicated all no-connects by a filled in circle.

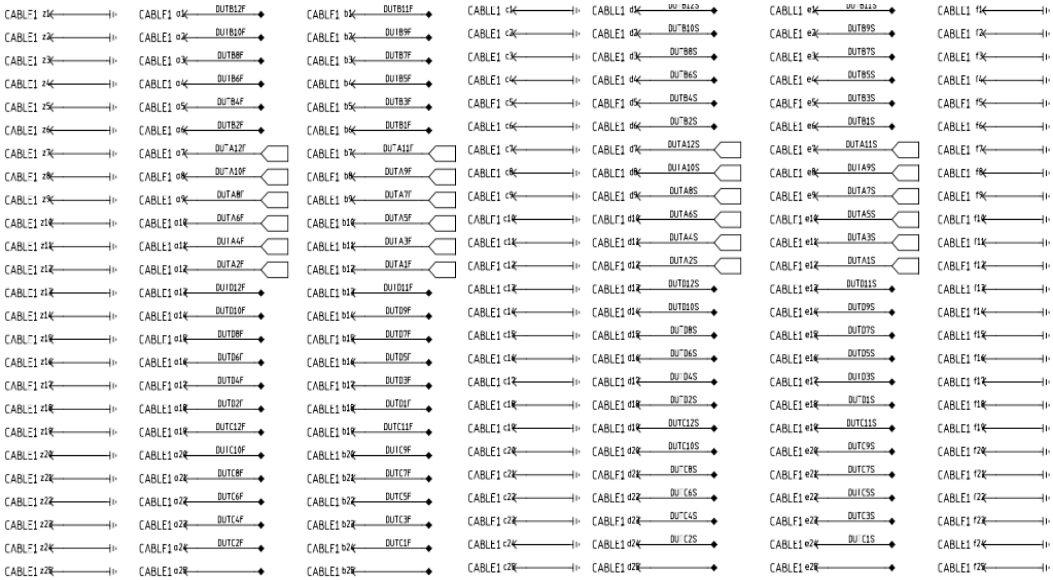


Figure 3: Joysignal Cable/Connector Pinout

Furthermore, while this should still condense all of the relevant connections to a single site output, lab continuity testing indicated that the schematic was either mislabeled or incorrectly designed. The provided cable does have the ability to be inserted "backwards," but the screw terminals do not line up, making the operator unable to secure the connection. This is actually how the cable must be inserted in order to align the output pins to output on a single site. The row of unnamed pins along the very bottom row of the connector (row z, in the cable pinout) actually appear on the top row of the connector, offsetting all of the output rows by 1 when the cable is inserted correctly (that is, the screw terminals line up), and pushing an entire row of outputs onto a different site. This corrected structure is illustrated below, where original labels are in parenthesis, and the numbers in the boxes indicate the corresponding pin on each DSUB connector.

	Z (F)	A (E)	B (D)	C (C)	D (B)	E (A)	F (Z)
1 (25)	GND	1	2	GND	14	15	GND
2 (24)	GND	3	4	GND	16	17	GND
3 (23)	GND	5	6	GND	18	19	GND
4 (22)	GND	8	9	GND	20	21	GND
5 (21)	GND	10	11	GND	22	23	GND
6 (20)	GND	12	13	GND	24	25	GND
7 (19)	GND	13	12	GND	25	24	GND
8 (18)	GND	11	10	GND	23	22	GND
9 (17)	GND	9	8	GND	21	20	GND
10 (16)	GND	6	5	GND	19	18	GND
11 (15)	GND	4	3	GND	17	16	GND
12 (14)	GND	2	1	GND	15	14	GND
13 (13)	GND	13	12	GND	25	24	GND
14 (12)	GND	11	10	GND	23	22	GND
15 (11)	GND	9	8	GND	21	20	GND
18 (10)	GND	7	5	GND	19	18	GND
17 (9)	GND	4	3	GND	17	16	GND
18 (8)	GND	2	1	GND	15	14	GND
19 (7)	GND	1	2	GND	14	15	GND
20 (6)	GND	3	4	GND	16	17	GND
21 (5)	GND	5	7	GND	18	19	GND
22 (4)	GND	8	9	GND	20	21	GND
23 (3)	GND	10	11	GND	22	23	GND
24 (2)	GND	12	13	GND	24	25	GND
25 (1)	GND	NC	NC	GND	NC	NC	GND

SITE 1
SITE 2
SITE 3
SITE 4

Figure 4: Corrected Joysignal Cable Pinout

For this board to work well and all of the outputs to go to a single site with the given cable, the cable itself must be inserted to where the screw terminals do not line up (backwards). In this case, the output was focused to one female DSUB labeled “SITE 1.”

A semester of testing classes did attempt to use this setup, but with little to no success. It was simply too complicated of a setup to justify the means, especially with an odd type of cable connection and a cable that cannot be secured into place. Other lab concerns were the inability to screw down the cable (limiting the overall lifetime of the connector and opening the door to tampering) and cost/complexity of making another cable (the connector appears to have been discontinued by the manufacturer).

2.2.2 Relay System

One may wonder how SMU and HSDIO outputs – where the latter has at least 24 output channels – can condense to a single 25-pin DSUB. The answer is a clever relay system implemented with Pickering 107-Series Mini-SIL Reed Relays, where the user can switch between use of the HSDIO and SMU.

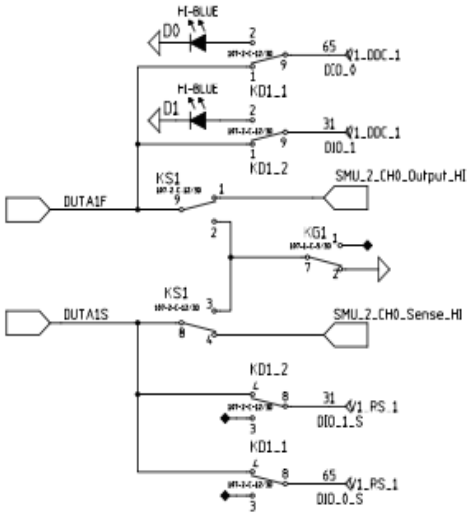


Figure 5: Original Switching System

The use of Double Pole-Double Throw (also known as DPDT or 2 Form C) relays allow the operator to use a single switching operation to change both output (DUTA1F in the figure) and sense (DUTA1S) relays, eliminating a potential error in forgetting to switch over the sense pin when the output is switched. This idea also saves board space by reducing the number of parts. Further along in the relay system, a bank of 24 LEDs can be accessed via the HSDIO output, to be used as a demo of multisite testing or just to debug the relays and the HSDIO.

However, several issues were noticed from a design standpoint. No current limiting resistors were used on the LED bank, apparently assuming that the instrumentation would internally limit current output, even though this is highly discouraged in device manuals [5][6]. Also with this setup, it is completely possible to have both the HSDIO and SMU driving separate voltages while they are still connected. This could cause an array of problems, the most dangerous being potentially "shorting" a reference (if the HSDIO is driven to a logic voltage and the SMU is driven to 0 V and unintentionally sinking current). The lab should not have to rely on the instrument's current limiting software to catch this and save the instrumentation. This is especially dangerous when use of the system is often students learning the software for the first time.

Also, in the case of reproduction of the board, reed relays are certainly one of the best choices for small signal testing, but they are notoriously expensive. Pickering does not release online pricing for their relays, but Coto Technologies relays of similar specifications were listed at $20.16 per relay [8]. As there are exactly 48 relays on the donated load board, reproduction cost of just the relays is over $800 (even when using the 10-piece discount of $17.92 each).

2.2.3 Single SMU Output

Another immediate concern came in the form of using a single SMU. If three SMUs were connected to the load board, it would be completely possible to access an SMU from any pin on the output site. However, as it stands, only one SMU means that the outputs could be sporadically placed and most output pins would not have access to an SMU pin. Any daughter card designed to connect to the DSUB output would have to take this into consideration.

While several solutions presented themselves – such as purchasing two additional SMUs or placing one of the modules from the old chassis into the STS – not many were practical from a cost or long-term solution standpoint. PXIe-4140s, which are what this load board was originally designed for, sold for over $5,000 each at the time this research was done [6]. The other PXIe-4140 unit housed in the PSPE lab was already in use on an existing test chassis. By placing it into the STS, students would lose test capabilities on the other station. Of all the considerations that had to be taken into account, this particular issue needed to be the most cost-effective.

CHAPTER III

REDESIGN OF THE LOAD BOARD

The largest overhaul of the system included an entire redesign of design interface board, otherwise known as the system load board. The problems listed in the previous chapter were simply too great to overcome to consider long-term system use of the original equipment. A new load board also presented a host of advantages – including the ability to tailor design to the needs of the PSPE lab.

3.1 Considerations

While the donated load board had some insurmountable issues, there were several ideas that were given consideration in the new design. The 24 HSDIO LEDs, shaped into the logo of NI and documented below, provided an excellent debug and demo tool that many students use when learning or teaching the relay system. The addition of current limiting resistors satisfies all potential problems with the LED layout. Also, if the number of LEDs was kept consistent, it would be possible to still use the LED multisite demo that was given with the STS load board with no coding modifications.

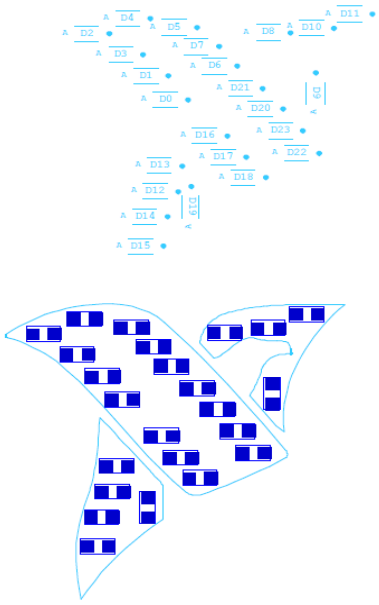


Figure 6: Original LED Layout

Because the relays were chosen to run off of the PXI-2567 Relay Driver's internal 5V and 12V rails, indicator LEDs appeared on the original design to indicate the status of

these power rails. The fuses within the relay driver, as the lab has most recently found out, are extremely sensitive, and status LEDs make it easy to pinpoint relay issues in the case of a power rail failure. For the redesign, it was decided to keep the 5V and 12V power rails, and the status LEDs were placed on the top of the load board instead of the bottom. This is so students do not have to open the clamshell and risk pulling a cable in an attempt to see if the power rails are active. Decoupling capacitors were also included from the original design.

An attempt was made to determine if the original design included separate analog and digital grounds, but the board design files given to the lab were incomplete and appeared to only show the footprints for the connectors, instead of the actual PCB layout. Also, PCB thickness appears much greater than the standard 0.062 inch (the number appears as "3 MIL" on the dimensions file, but it would be more plausible this was intended as 3 mm, or 0.118 inch). From this, one can assume that the PCB layout was greater than 12 layers. The choice of layer count and setup for any new design had to be carefully considered, as the HSDIO can drive signals up to 200 MHz [5]. This is discussed in detail under the PCB section.

Lastly, all instrumentation connectors had to be maintained. The PXIe-4140 SMU has a 25-pin DSUB output cable [6], the PXIe-6556 HSDIO has two 68-pin VHDCI output cable [5], and the PXI-2567 Relay Driver has a 78-pin High Density DSUB output cable [9]. Because only a single SMU was planned for the new design, two connectors were eliminated from the original design and opened up room on the board for potential switching modules that could expand the output of the SMU to more pins. The Joy Signal connector was replaced with several more common 25-pin DSUB connectors.

3.2 New Hardware

3.2.1 Selection of Switching Module

The bench top PXI system that the PSPE lab had before the arrival of the STS included a switch matrix that allows the operator to switch between SMU and HSDIO outputs in the code, allowing one pin access to any output on the SMU or HSDIO. An example of how the switch matrix connections work is indicated below.

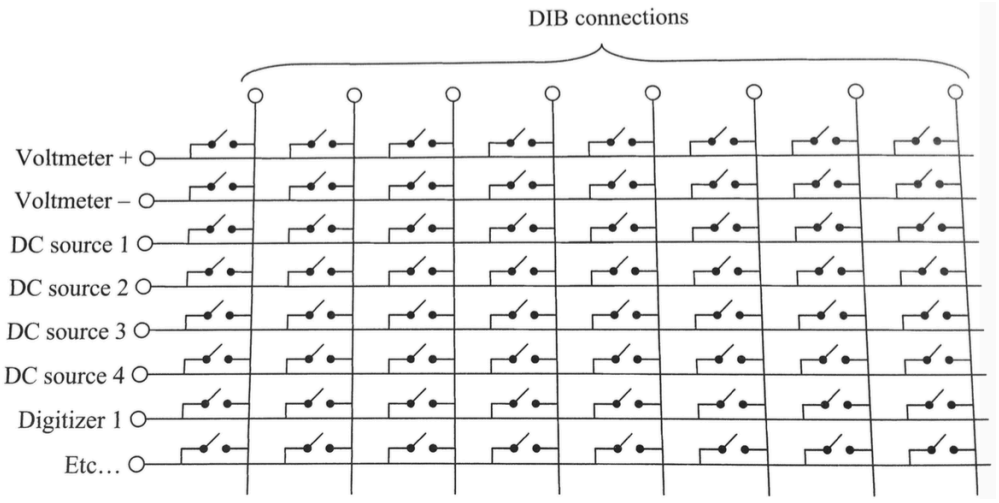


Figure 7: Switch Matrix Layout [3]

This switch matrix, however, was designed for an HSDIO that did not have a secondary VHDCI output, like the PXIe-6556 does for its sense outputs. National Instruments has not come out with another switch matrix specifically for this case, so any other switch matrix used would have to use the PCB to route signals from the VHDCI connectors to the switch matrix connectors.

Because the relay system will remain and allow students to switch between HSDIO and SMU instrumentation, only the SMU's four channels should be considered for expansion, given 4 outputs and sense, versus 24 outputs and sense on the HSDIO. Many switch matrices offer a 4 or 8 input dimension for the SMU, but dimensions for the output DUT side are on the order of 16 (PXIe-2529) and 32 (PXIe-2534 and PXIe-2532B). [10] These dimensions can be read as "8x16" in the case of the PXIe-2529 [10], which means 8 of the outputs from the SMU (4 channels of output and the 4 corresponding sense connections) can connect to one of any 16 connections on the other side, otherwise referred to as the DUT side. Other matrices exist for 4 and 8 input dimensions, but for 2-wire connectivity – ideal for use with SMUs that have output HI and LO pins, such as the PXIe-4140 [6] – these were the only three options available through National Instruments [10].

Another option in the switches category was to use a multiplexer configuration. Instead of allowing switching to any DUT pin, multiplexers can switch between channels

off of a common port. The illustration below is a single, 2-wire example of this setup [11].

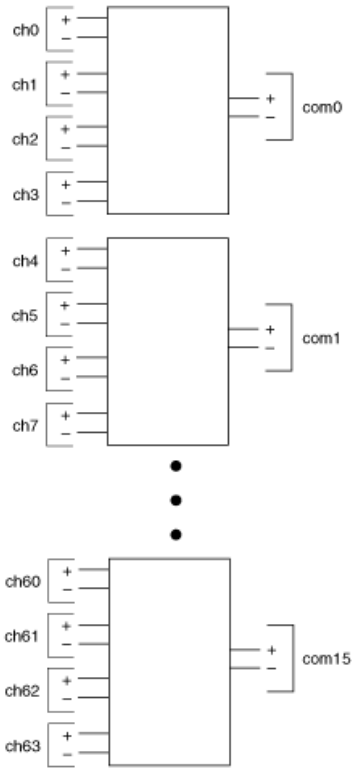


Figure 8: PXI-2567 MUX Layout [11]

With this design, access to the SMU's output can be expanded from 4 DUT pins to 16 DUT pins. Although some flexibility is lost through the multiplexer's inability to switch to *any* DUT pin, most devices tested in the PSPE lab do not require multiple power rails, and if they do, they are usually located on different sides of the packaging, such as an analog and digital supply on an ADC. More complex setups would certainly require custom daughter card design anyway, which can make sure not to position separate power rails on the same common port.

Multiplexers also have appeal in the pricing and future expansion categories. The PXI-2576 (128-Channel Multibank Multiplexer Module) retails for $1,704 alone [11]. In contrast, the least expensive switch matrix module, the PXIe-2529, retails for $2,307 alone, and connectivity to the SMU would consume all 8 channels on the smaller dimension [10]. The PXI-2576 has 16 banks of 4x1 2-wire multiplexers, with up to

100V/1 A switching capacity [11], which means the PXIe-4140 SMU would only take up half of the banks and would not come close to the current limitations [6]. This opens the door for future expansion of the system's power capabilities with a higher power SMU.

Ultimately, the decision was made to add the PXI-2576 to PSPE's STS system as the switching module. The LFH160 cable terminates into four 50-pin DSUB connectors [12], and if only half of the banks are in use, only two connectors are required on the load board. The modified connectivity diagram below shows how multiplexer output can work in respect to the lab's system. The default position of the MUX is a no-connect and can be modified using National Instrument's included Switch Executive software, either through a "Soft Front Panel," which gives the user a graphical interface, or programmatically through LabVIEW drivers using NI Switch software.

SMU CH0	COM0	CH0		SMU CH2	COM4	CH16
		CH1				CH17
		CH2				CH18
		CH3				CH19
SMU CH0 SENSE	COM1	CH4		SMU CH2 SENSE	COM5	CH20
		CH5				CH21
		CH6				CH22
		CH7				CH23
SMU CH1	COM2	CH8		SMU CH3	COM6	CH24
		CH9				CH25
		CH10				CH26
		CH11				CH27
SMU CH1 SENSE	COM3	CH12		SMU CH3 SENSE	COM7	CH28
		CH13				CH29
		CH14				CH30
		CH15				CH31

Figure 9: SMU - MUX Connectivity

3.2.2 Choice of Relays

As stated in section 2.2.2, Pickering 107 Series reed relays were used in the donated load board, adding up to a cost that was simply not justifiable to reproduce. A search for similar, lower-cost relays began. Several initial requirements were that they be of DPDT design, the ability to run off of the relay driver's provided 12 V or 5 V power

supplies, and not break the fuses on those supplies (2 A for the 5 V, 0.75 A for the 12 V) when all coils are driven [9]. Since the relay driver is, put simply, a switch system that connects the path to ground when the common and channel ports are connected via software triggers, it can work with almost any set of small signal relays [9].

Electromechanical relays often offer a more cost efficient solution to reed relays, although some drawbacks, such as more limited operating lifetimes and particulate buildup over time that sometimes requires a minimum switching capacity. This minimum switching capacity is specified because, over time, contacts on the relay can build up particulates that need a minimum voltage or current in order to "burn off" this build up upon activation [13].

Even advertised low-signal relays, such as Omron's G5V-2, require a "minimum permissible load" of 10 μA [14]. For low-power logic gates, such as the SN74HC00 mentioned previously, testing on input currents could run as low as 1 μA [7]. If tests were to commence on relays like the G5V-2, any low input current and voltage testing could be extremely inaccurate, so it was important to select a relay where this would not be an issue.

This solution came in the form of TE Connectivity's Axicom V23079 series relays. This series of relays include variations for both 5 V and 12 V coils [15]. The only minimum specification given is minimum switching voltage, which is 100 μV, is entirely sufficient when testing with the PXIe-4140 and the PXIe-6556, because typical logic voltage testing does not require precise readings under 100 μV [5][6][15]. The table below lists some comparisons, particularly in the coils, of the original and proposed new relays. Interestingly enough, the Axicom Relays appear to be more robust in current carrying and switching voltage capacity, even though they are much less expensive than their Pickering counterparts.

Table 2: Axicom and Pickering Relay Comparison [15][16]

	TE Axicom v23079a	Pickering 107C Series
Relay Type	Electromechanical	Reed
Arrangement	DPDT (2 form C)	DPDT (2 form C)
Coil Voltage	5 V, 12 V	5 V, 12 V
Coil Power	140 mW	67 mW (5V), 144 mW (12V)
Max Contact Resistance	<0.050 Ω	0.22 Ω
Max Carry Current	2 A	1.2 A
Max Switching Volts	220 VDC	200 V
Min Carrying Capacity	100 µV	N/A

It appears that the noticeable disadvantage to this series is the loss of slim, in-line structures that were seen with the Pickering relays. However, as the board dimensions were set at 16.4”x8.2”, it was clear that enough board space was present to accommodate the same number of relays as present on the donated load board. The Axicom relays also boast a low profile and are slimmer than traditional relays [16]. Below are the custom footprints and custom part design, versus the data sheet specification.

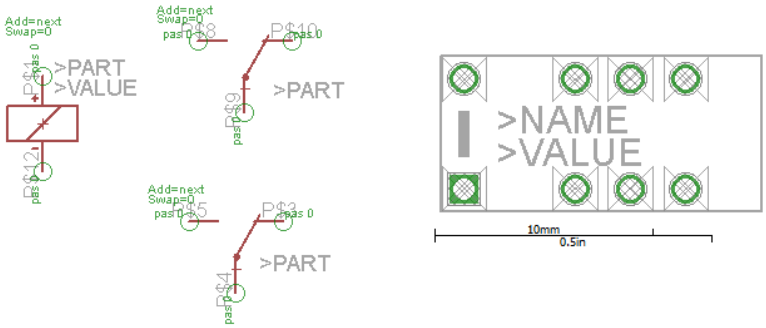


Figure 10: V23079a Relay Symbol and Footprint

3.3 Schematic Design

EagleCAD was the chosen design platform, due in part to Texas Tech’s professional licensure of the software. The professional version provides a lot of flexibility in large designs, especially with a design that has few traditional circuit elements and several high-density connectors.

3.3.1 Determining Output Structure

Before any schematic element was put into place, a detailed list of inputs versus outputs had to be documented. Datasheets were collected for each piece of equipment and connector parts were added into Eagle's part libraries. A specific part library was created and distributed to participating lab students in order to provide these renderings for any student interested in information on designing another custom load board.

The next page is a figure that illustrates the custom connector layouts designed in EagleCAD for the HSDIO DDC Output VHDCI connector. Other custom connector layouts created for this project can be found in Appendix A.

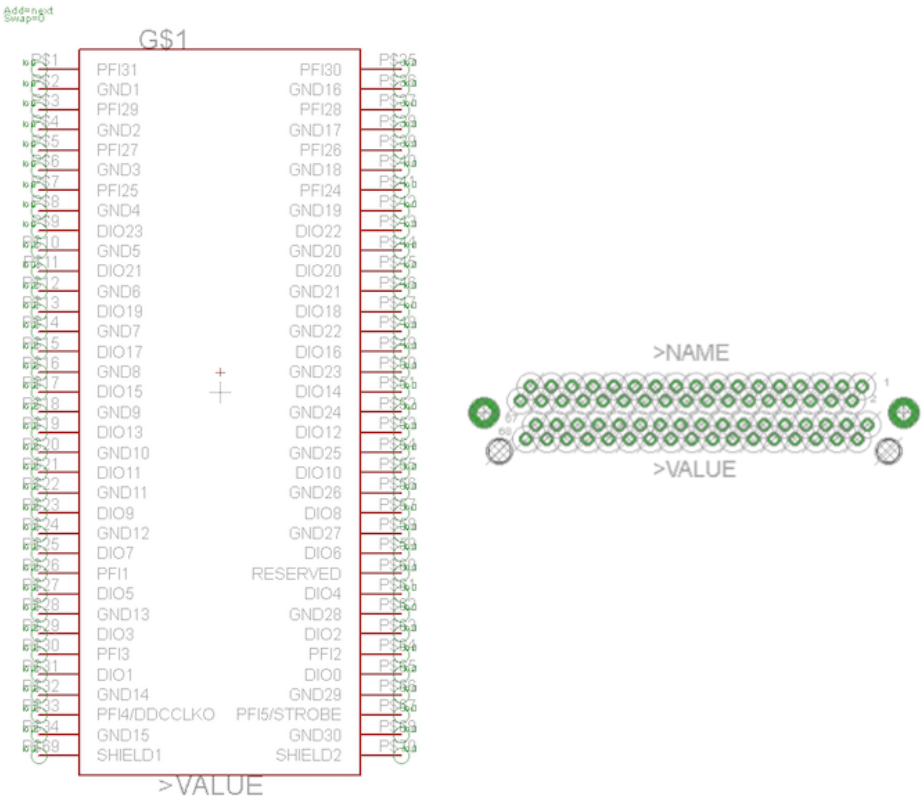


Figure 11: HSDIO-DDC Custom Connector Layout

The other HSDIO connector, the VHDCI "sense" connector, has the same VHDCI 68-pin footprint as the DDC connector, but required a separate schematic image that linked the sense lines to individual pins on the connector. Similarly, the multiplexer

(MUX) required four different connector layouts for each of the four 50-pin DSUB connectors.

Once all channels from the instrumentation were laid out, and desired outputs arranged in a preferred order onto the load board, they had to be split into several 25-pin DSUB connectors. This connector was chosen due to its wide availability and cost effectiveness. Students can, quite easily, make their own daughter card designs based on this connector's output. A table of the proposed output structure is below.

Table 3: New DSUB25 Output Structure

Pin	OUTPUT 1	OUTPUT 2	OUTPUT 3
1	DIO0/CH0 (1) HI	DIO8/CH2 (1) HI	DIO19/PFI1
2	DIO0/CH0 (1) HI SENSE	DIO8/CH2 (1) HI SENSE	DIO19/PFI1 SENSE
3	DIO1/CH0 (2) HI	DIO9/CH2 (2) HI	NC
4	DIO1/CH0 (2) HI SENSE	DIO9/CH2 (2) HI SENSE	NC
5	DIO2/CH0 (3) HI	DIO10/CH2 (3) HI	DIO18
6	DIO2/CH0 (3) HI SENSE	DIO10/CH2 (3) HI SENSE	DIO18 SENSE
7	DIO3/CH0 (4) HI	DIO11/CH2 (4) HI	GND
8	DIO3/CH0 (4) HI SENSE	DIO11/CH2 (4) HI SENSE	GND
9	DIO4/CH1 (1) HI	DIO12/CH3 (1) HI	DIO22/PFI4
10	DIO4/CH1 (1) HI SENSE	DIO12/CH3 (1) HI SENSE	DIO22/PFI4 SENSE
11	DIO5/CH1 (2) HI	DIO13/CH3 (2) HI	DIO23/PFI5
12	DIO5/CH1 (2) HI SENSE	DIO13/CH3 (2) HI SENSE	DIO23/PFI5 SENSE
13	GND	GND	GND
14	DIO6/CH1 (3) HI	DIO14/CH3 (3) HI	GND
15	DIO6/CH1 (3) HI SENSE	DIO14/CH3 (3) HI SENSE	PFI26
16	DIO7/CH1 (4) HI	DIO15/CH3 (4) HI	PFI27
17	DIO7/CH1 (4) HI SENSE	DIO15/CH3 (4) HI SENSE	PFI28
18	GND	GND	PFI29
19	GND	GND	PFI30
20	GND	GND	PFI31
21	PFI25	PFI24	NC
22	DIO16	DIO20	NC
23	DIO16 SENSE	DIO20 SENSE	NC
24	DIO17	DIO21	NC
25	DIO17 SENSE	DIO21 SENSE	NC

When the HSDIO and SMU inputs are accounted for in the relay system (the "/" indicates a relay to switch between, and the number in parenthesis is the switch position of the multiplexer when wanting to access the SMU on that pin), the number of DSUB connectors that must be used totals to three, where two output cables have almost identical structures, and one can be considered to have "auxiliary" lines, such as additional HSDIO and Relay Driver controls that lie beyond the scope of many testing projects.

3.3.2 Relay Structure

The relays, in their default, "off" states, are to be set to output all HSDIO lines to the cable, much like they did in the original design. The PXI-2576 relay driver, via Switch Executive, must be used in order to switch the relays to the LED position, or for the multiplexer to provide SMU access. This was designed so that testing with the HSDIO can be immediately set up. An image of the new design's relay system is shown below. Because switching to the LED ties up the DIO channel, the DIO sense line is not used in this situation.

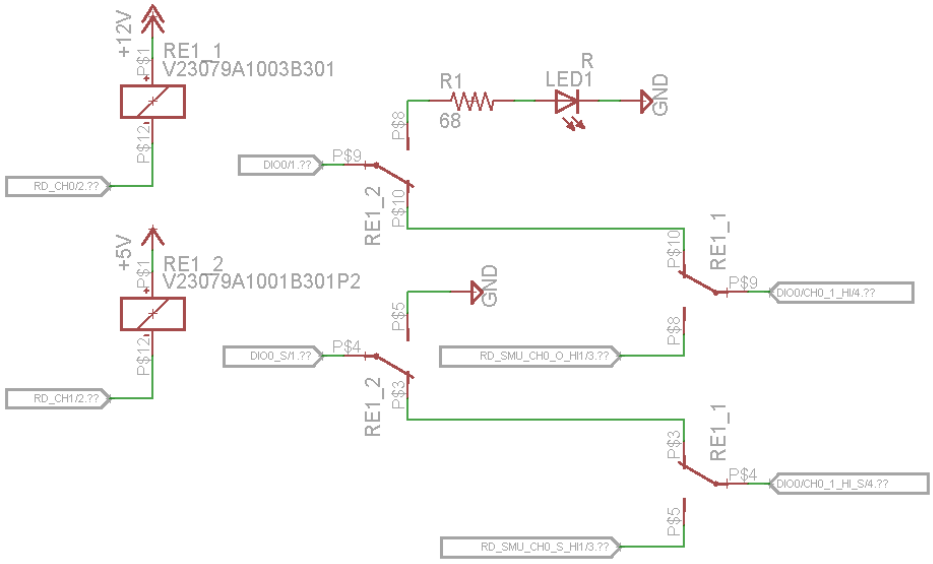


Figure 12: HSDIO-SMU-LED Double Relay Structure

This output differs from the original in that it took out ground relays – as setting the HSDIO or SMU to drive "0 V" works well as a ground reference – and narrows each DIO channel and LED to a single system, instead of in the previous design, where two LEDs and two DIO channels were unnecessarily included off of a DUT cable output.

Two types of relays can also be seen in use: the 5 V and 12 V variations of the V23079a [15]. This was designed so that, when all the relays have been activated, the total current will not overload one of the power rails off of the relay driver [9]. By the final numbers, there are twenty-four 5 V relays, and twenty-one 12V relays. The three extra 5 V relays are found in switching between DIO lines that do not have a corresponding SMU or PFI line to switch to, but can be changed to an LED (this is for

DIO channels 16-18, so the DIO channels remained in numerical order for the LEDs). An example of this is shown below.

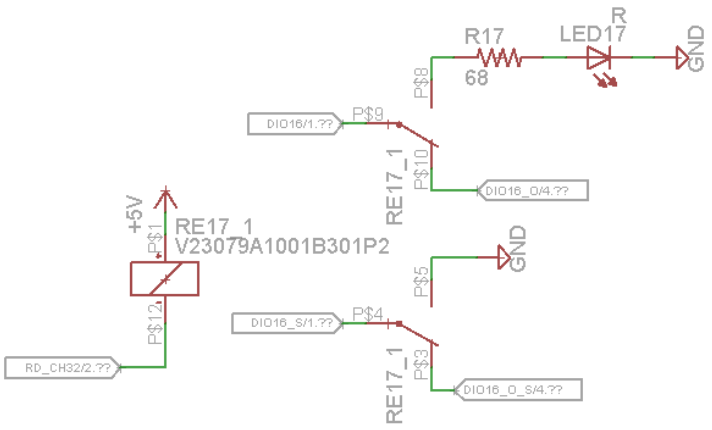


Figure 13: HSDIO-LED Single Switching Relay

Use was split between the two voltage levels in order to not overload the power rails provided by the relay driver. For instance, twenty-one 12 V relays, at a rated coil resistance of 1029 Ω, requires about 11.67 mA of current when a single relay is activated [15]. If all twenty-one are active, then the 12 V rail must be able to supply about 245 mA of current, well under the 750 mA maximum on the fuse [9]. On the 5 V side, that fuse can hold on a supply up to 2 A of current [9]. The coil resistance of the 5 V relays is stated at 178 Ω, for an on-state current of about 28 mA per relay [15]. At twenty-four relays all active (in the case of engaging use of all the LEDs), this requires at least 674 mA.

The common, encouraged use of the LEDs was why the 5 V relays, and the higher-current 5 V rail, were chosen to switch the DIO channels between the LED and connector outputs. Even though both types of relays have the same coil power consumption, there are still more relays required to switch over to the LEDs (25 relays) than there are for switching to SMU or PFI line outputs (20 relays).

3.3.3 Miscellaneous Elements

Aside from the relay structure, the load board otherwise must be kept simple and straightforward for new student use. The only additional elements outside of the connector routes were several decoupling capacitors off of the HSDIO cable shielding,

decoupling capacitors for the power rails, and the power rail indicator LEDs and resistors. These elements are found on the last page of the schematic, shown below.

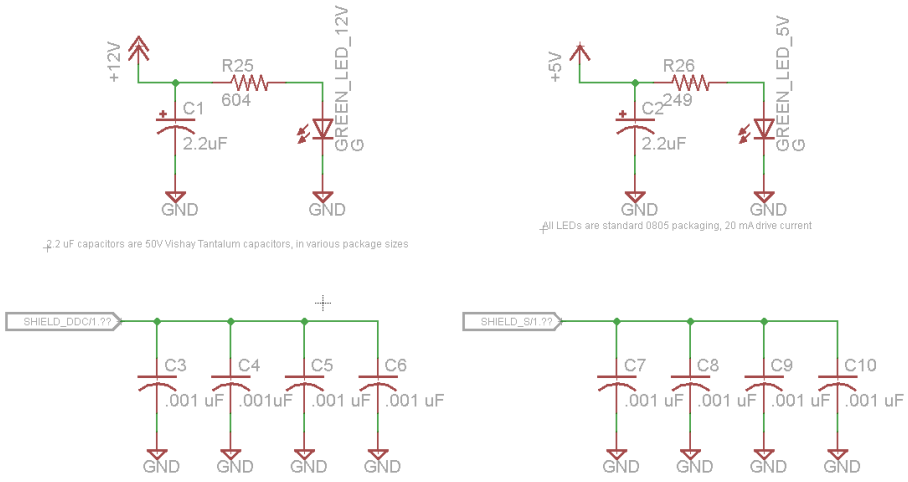


Figure 14: Additional Schematic Elements

3.4 PCB Design

Access to the original design was not immediately available to the lab, so some research had to be done in order to decide new board specifications. While some decisions had to be left to trial and error, others were more concrete, such as placement of screws and clearances so the new load board will fit onto the STS clamshell in the same way the original did.

3.3.1 Dimensional Outlines

Exact dimensions and placement of screw holes on the original boards were provided in dimensional drawings for the STS. These extraneous images can be found in Appendix A, and were the basis for the new dimensional designs. Care had to be taken in order to include clearance for the clamshell's large screws on the outer perimeter of the board, because EagleCAD does not encourage altering the original rectangular board shape. The solution to this was with the addition of four semicircles (the 5mm radius of which was specified in the original documentation) in the dimensional layer of the PCB layout.

Most companies did recommend including this cutout shape on the dimensional layer, and also noting this in a specifications document that these shapes were intended for cutout. It was not recommended to just use a drill hole, because the software generated errors that a drill appeared outside of board perimeter.

3.3.2 Signal Routing

Very few circuit components other than the relays were used for the final board layout, because adequate testing would require effective shorts between output points and instrumentation. To keep the voltage drop, no matter how small, across the traces, priority had to be given to HSDIO and SMU signals that were to be routed out to the output connectors to keep trace lengths short.

Connector placement also played a role in minimizing trace lengths. The image on the next page is the illustration of connector placement, which gave preference to HSDIO and SMU signals, while pushing the relay driver connector and LED bank circuitry off of the side, because LED route length is one of the lowest priority signals within the PCB.

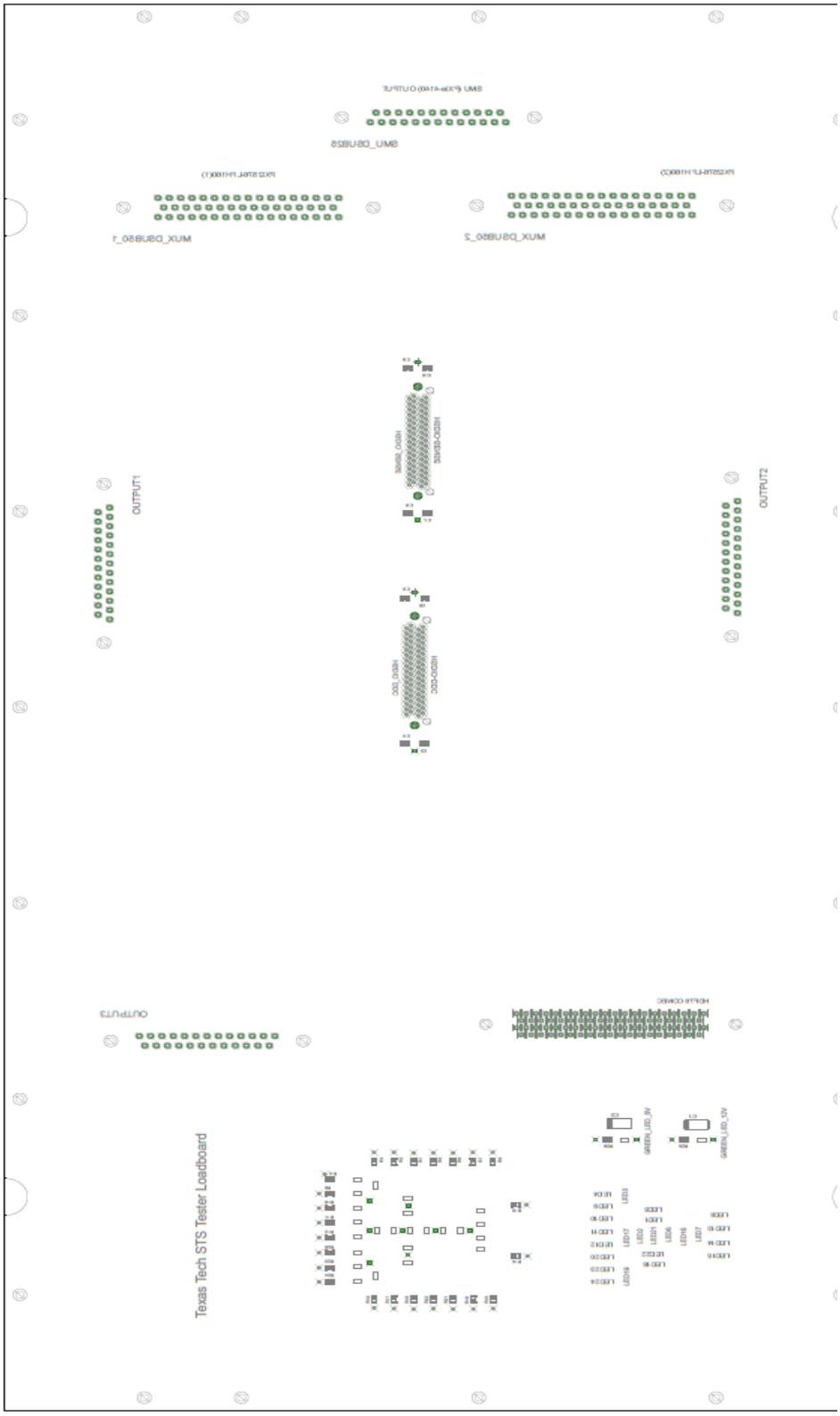


Figure 15: PCB Connector Layout

When dealing with a board over 16 inches long, it was quite easy to put down long traces without realizing it. The final layout took a few attempts at trial and error routing to observe the best possible placement of the connectors.

Another consideration is the use of larger trace, which makes for less of a voltage drop across the signal. There are several online resources that offer immediate calculations of PCB trace properties (in order to determine optimal trace widths), but the most common equation is: [17]

$$R = \rho \frac{L}{h \cdot W}(1 + t_C(t - 25)) \quad (1)$$

Where resistance R is determined by resistivity of copper, ρ (1.7×10^{-6} Ω-cm) multiplied by length of trace, L (cm), divided by trace height, *h* (cm), multiplied by trace width *W* (cm), and at room temperature (*t*=25°C), the temperature coefficient t_C (0.004041 per degree Celsius for copper) has no bearing on the result [17]. Furthermore, as temperatures in the lab do not fluctuate more than 5°C from room temperature, a swing of that magnitude in either direction would only affect the scale of 1 by 0.02 in either direction. For all preliminary calculations, room temperature was assumed.

When considering SMU maximum current output of 100 mA, a standard 1 oz copper weight (0.0035 cm thickness), 10-inch long, 12-mil trace at this current will only produce a voltage drop of 48 mV. For the HSDIO, a maximum current of 35 mA on a 10-inch trace with the same thickness characteristics at a narrower 10-mils will produce a voltage drop of 33 mV. For the final layout of the board 10-12 mil traces were used in all cases except for immediate outlets of the VHDCI connectors, shown below.

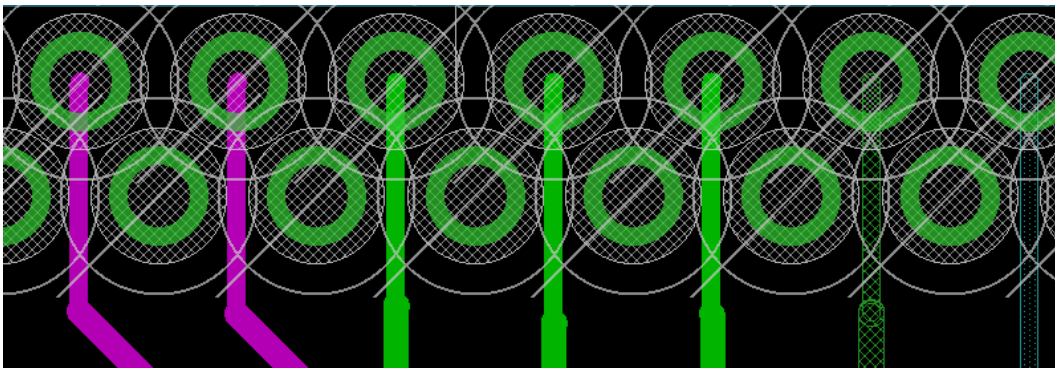


Figure 16: VHDCI Connector Issues

In this instance, 7 mil traces had to be used to provide sufficient clearance (greater than 6 mils) between the pads of the connector and the traces themselves. They were expanded upon reaching free board space. The only caveat of this method is that smaller trace widths have more power losses [17], but given that the HSDIO's maximum current output is 35 mA, the voltage drop across the long 10-mil section of the trace is already negligible, so a much smaller section of 7-mil trace will not dramatically affect that.

After final design of the board, EagleCAD has a very useful tool for this type of calculation – trace properties of total length, maximum carrying current and frequency – by using the 'run length-freq-ri' command on the command line. This prevents the designer from having to collect all trace properties to satisfy Equation 1 in order to verify trace properties on every signal. A small sample is seen in the figure below.

Cu thickness = 0.035 mm

Signal	f max. [MHz]	l [mm]	A [mm2]	R [mOhm]	w min [mm]	w max [mm]	Imax [A]
DIO1	3654.06	82.046	0.009	160.58	0.254	0.254	0.80
DIO1/CH0_2_HI	5017.17	59.755	0.011	97.46	0.305	0.305	0.95
DIO1/CH0_2_HI_S	5362.30	55.909	0.011	91.19	0.305	0.305	0.95
DIO1_S	7501.99	39.963	0.009	78.22	0.254	0.254	0.80

Figure 17: EagleCAD Trace Properties Viewer

By following the DIO1 channel from the HSDIO to the relay system (DIO1) and from the relay system to the output (DIO1/CH0_2_HI), one can interpret a very close estimation of voltage drop across each line. In this case, the total line length is 141.801 mm (or 5.58 inches) for a total resistance of 258.04 mΩ. At the maximum output current of 35 mA from each DIO channel, the maximum voltage drop across the trace would be ~9 mV maximum. This voltage is negligible with tests designed to confirm what is off of a datasheet of logic ICs, like many final projects found in the testing classes [7]. This

type of parameter would only need to be taken into account during device characterization, which is of a much more advanced structure.

Many other routing aspects can be checked programmatically. Spacing between traces was suggested to be at least twice of the trace width, so 12 mil traces required 24-mil spacing, and 10 mil traces requires at least 20-mil spacing. This can be checked in EagleCAD's own DRC check. If the check on the final design is set to have minimum spacing of 20 mils, no errors arise, and when the minimum spacing is set to 24-mils, the only errors that appear are for trace widths of 10-mils, which already passed the 20-mil spacing check.

3.3.3 Layer Stack-up

The layer stack-up can dramatically affect the board specifications and also the overall cost of the board's fabrication. While most testing applications in PSPE do not typically require the fast signal generation from the HSDIO (even clock rates of the ADCs available in the lab are usually in kHz), the board design should still consider this prospect, so future projects with high speed applications do not require the order of a special load board.

Due to this, the high-speed digital signal layers should be separated from the potential analog SMU signals whenever possible. Most mixed-signal PCB designers recommend outside board layers be reserved for routing analog signals, and internal routing layers – sandwiched between power planes – be reserved for any high speed signals, due to the different ground return paths that the signal sets take [18]. Internal layers come in pairs of two, sandwiched between ground and power planes, where overlapping signals should be routed orthogonally (or perpendicularly) to the other [18][19]. The figure below is an example on an HSDIO layer pair.

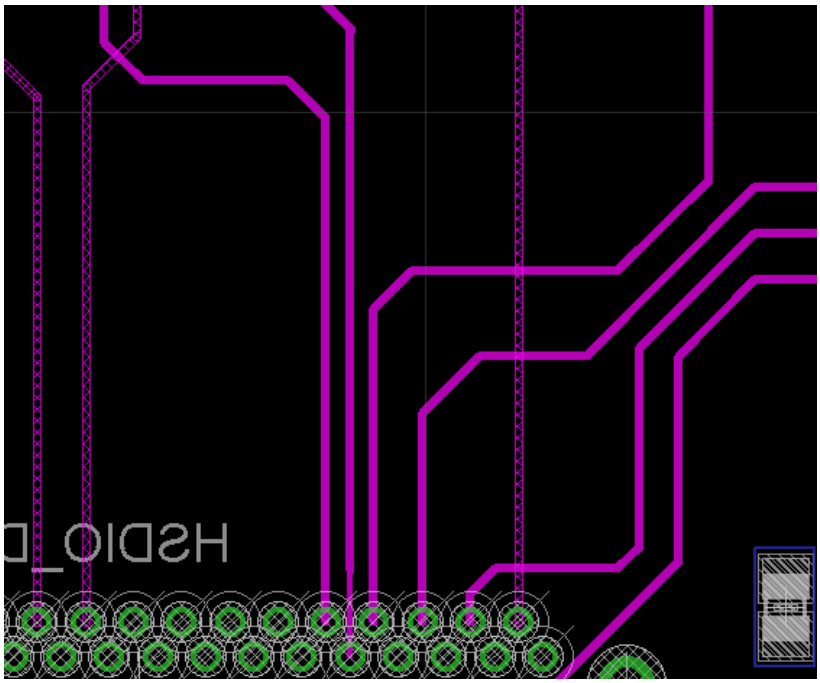


Figure 18: Orthogonally Routed Signal Example

Some costs were also able to be eliminated by avoiding the use of blind or buried vias. While original designs did try to use vias in an attempt to have inner signals switch layers (to possibly limit the layer count), the design still had to go with 8 signal routing layers for clean routing. Careful consideration during the design phase was able to eliminate all vias between inner layer signals. The only exception to this was found in the high-density connector for the relay driver. That design simply required some top and bottom layer vias to inner layers in order to let all channels be routed properly.

After some experimentation with an 8-layer design, it was eventually decided to increase the layer count to 12. With the use of high-speed signals, the only difference between an 8 and 10 layer board is the addition of two extra power plane layers [19]. 12-layer boards, on the other hand, add two more signal routing layers to the 10-layer design. The designated 12-layer stack-up is illustrated below, and based off of various stack-ups suggested by mixed-PCB designers [18][19][20]. While there was plenty of board space to accommodate signal routing, the high layer count is mostly to avoid the use of vias. The more vias used in the design, the more voltage drop each route potentially experiences, which, as stated in the previous section, could be problematic in lower voltage ranges [18].

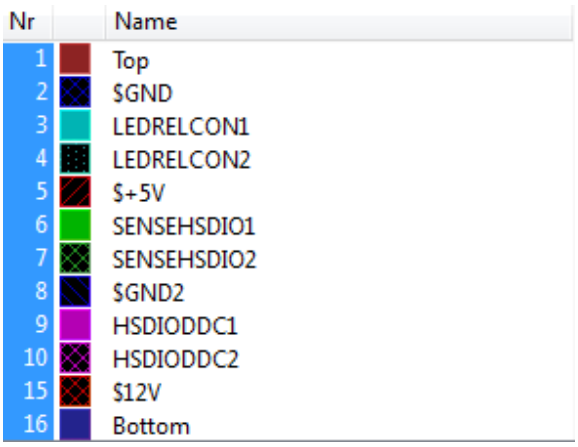


Figure 19: 12-Layer Stackup

This stackup offers the advantage of using 2 separate power planes – one for the 12 V and one for the 5 V plane for the relays. This is very useful, in that the power plane pins off of the relay driver's high density DSUB do not allow for easy use of large trace widths, as they are not located on outer edges. Mixed-signal PCB design rules also suggest solid, full-layer power and ground planes, as to provide adequate room for ground return paths for high-speed signals [18].

3.3.4 Final Board Specifications and Pricing

Although Texas Tech's Electrical Engineering department typically uses one company for student PCB orders, it became necessary to get custom quotes from other PCB fabrication facilities, as the original company proved to be twice as much as the competition for a board of this scale. Keeping in mind that component cost and board assembly were still part of the equation, turnaround time also became a factor.

Table 4: Competitive Quotes for STS Load Board

Company	Quoted Cost (2 units)
Advanced Circuits (4pcb)	$2,808.62
Bittele (7pcb)	$1,377.82
Epec PCB	$1,013.50

Each company listed was researched for competitive pricing and good customer reviews. Ordering two boards was a choice made due to only a slight (less than 10%) price increase while the STS is capable of holding two half-panel boards. Advanced Circuits is the company the university typically does business with, but was almost

double (or even triple) the typical quote by competitors, at twice the lead-time. The university uses this particular company due to their student discounts, but the sheer size of this board was too large to be included in their usual discount.

Bittele did have several impressive clients (Texas Instruments, Dell, Stanford University, etc.), [20] though, so even though they were slightly more expensive than Epec, they were the company chosen to manufacture the two boards. It should be noted that Epec's pricing included a $250 off first-order special that the website was running the week that the quotes were assembled, so had it not been for the discount, their pricing would have been very similar to Bittele [21].

The next table is a list of the final board specifications sent to the board fabricators. 12 layers is the largest number of layers one can design with a 0.062" standard thickness board [19]. Most other attributes follow standard PCB ordering information, although a red solder mask was chosen over green for aesthetic purposes.

Table 5: Final STS Tester Load Board Specifications

	Specification
X Dimension	8.2 inches
Y Dimension	16.4 inches
Thickness	0.062 inches
Material	FR4 (default)
Finished Plating	HASL (default)
Copper Weight (Outer)	1.0 oz
Copper Weight (Inner)	1.0 oz
Soldermask	Yes (red)
Silkscreen	Yes (both sides)
Smallest Trace Width	0.007 inches (7 mils)
Smallest Trace Spacing	0.02 inches (20 mils)
Smallest Via	0.019 inches (19 mils)

CHAPTER IV

AUXILIARY EQUIPMENT AND PROGRAM DEMOS

Documentation was a major issue that presented itself in past PXI projects, so care was taken to provide incoming students with as much material as possible to develop working tests. This included the design of daughter cards for the system, and also example code to utilize National Instrument's new Semiconductor Module add-on for TestStand.

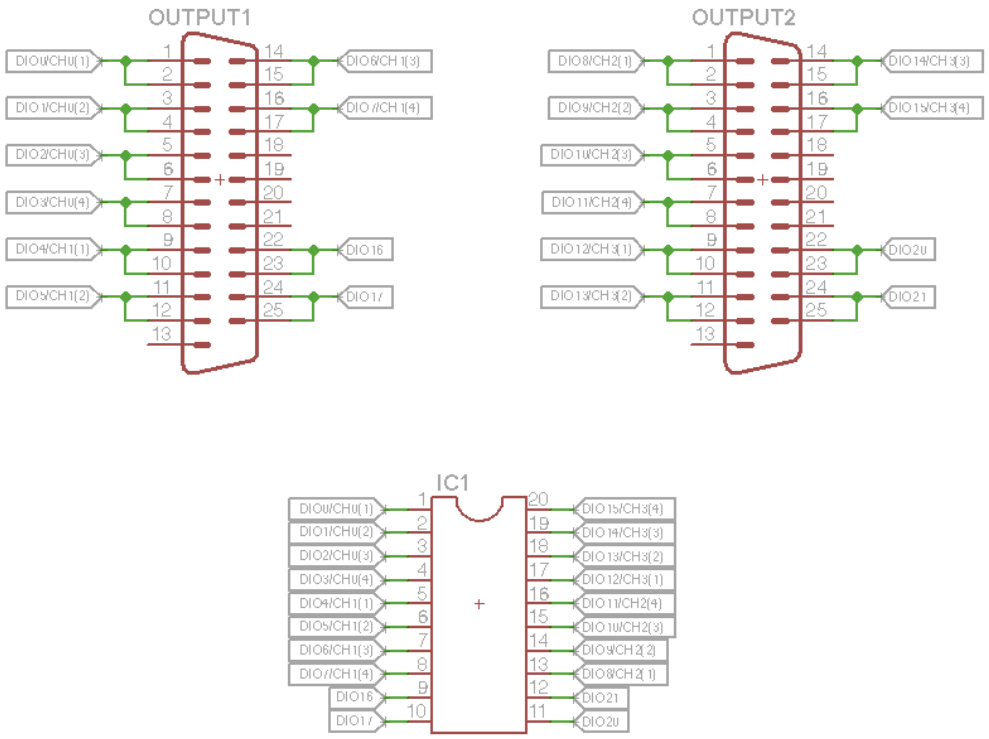
4.1 Daughter Card Designs

While several designs for daughter cards will be provided to students, it was beyond the scope of this project to design boards for very specific devices. Two particular board designs – a generic DIP socket for up to 20-pin devices and a connector breakout board – were chosen as the most important for total student use. It has been documented that students are welcomed and encouraged to design their own custom daughter cards through the department if they require a more specific design.

4.1.1 20-pin DIP Socket

Many simply DIP devices can be hosted in a 20-pin DIP socket, and it was observed that the vast majority of ICs used in the testing classes fell into the 20-pin DIP (or lower) category. 16-pin devices appear to be the most common design, but single DSUB cable outputs from the STS only offer up to 10 outputs per cable (due to the inclusion of voltage sense lines), which can be found back in section 3.3.1. Even for 16-pin devices, two output cables need to be used to accommodate all pins in as flexible of a way as possible. The figure below is the schematic design and PCB layout for this board.

(a)



(b)

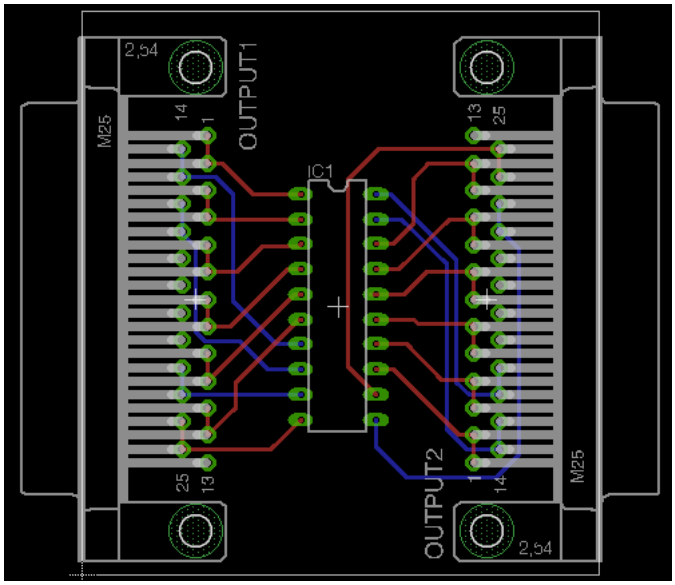


Figure 20: 20-Pin DIP Breakout Board (a) Schematic and (b) PCB Layout

Voltage sense lines must be shorted to the output lines. Use of sense lines is typical in industry, as they check for the voltage at the point of contact with the output line, and make sure that point is driven to the correct voltage via the output. However,

because this system relies on so many long traces and two cable connections, the sense lines are included only for learning purposes.

One may also wonder why the socket does not connect directly to any of the cable's ground pins. This was to accommodate as many devices as possible within the DIP socket, and the position of the ground pin is difficult to predict between IC series and manufactures.

Because the bottom 4 pins do not include SMU connectivity, devices that require an SMU input (specifically, through V_{CC} and GND), should be 16-pins or less for use with this board. For example, a device off of TI's 7400 digital logic series has a V_{CC} pin in the upper right hand corner and a GND connection in the bottom, left hand corner. [7] If the SMU is used to connect V_{CC}, it would also be good practice to drive 0 V to GND from the SMU as well. In 20 pin devices, pin 10 does not have connectivity to an SMU through this board, so students should consider this when choosing devices to test.

4.1.2 Cable Breakout Board

For students that wish to prototype more complex designs, a breakout board from the cables need also be included in the designs. Although the jumper and potential use with a breadboard could cause some inaccuracies, this could be very useful when testing new devices, and could lead to new daughter card designs for more complex devices that require the use of the HSDIO's PFI lines or higher I/O ICs. The suggested board layout is illustrated on the next page.

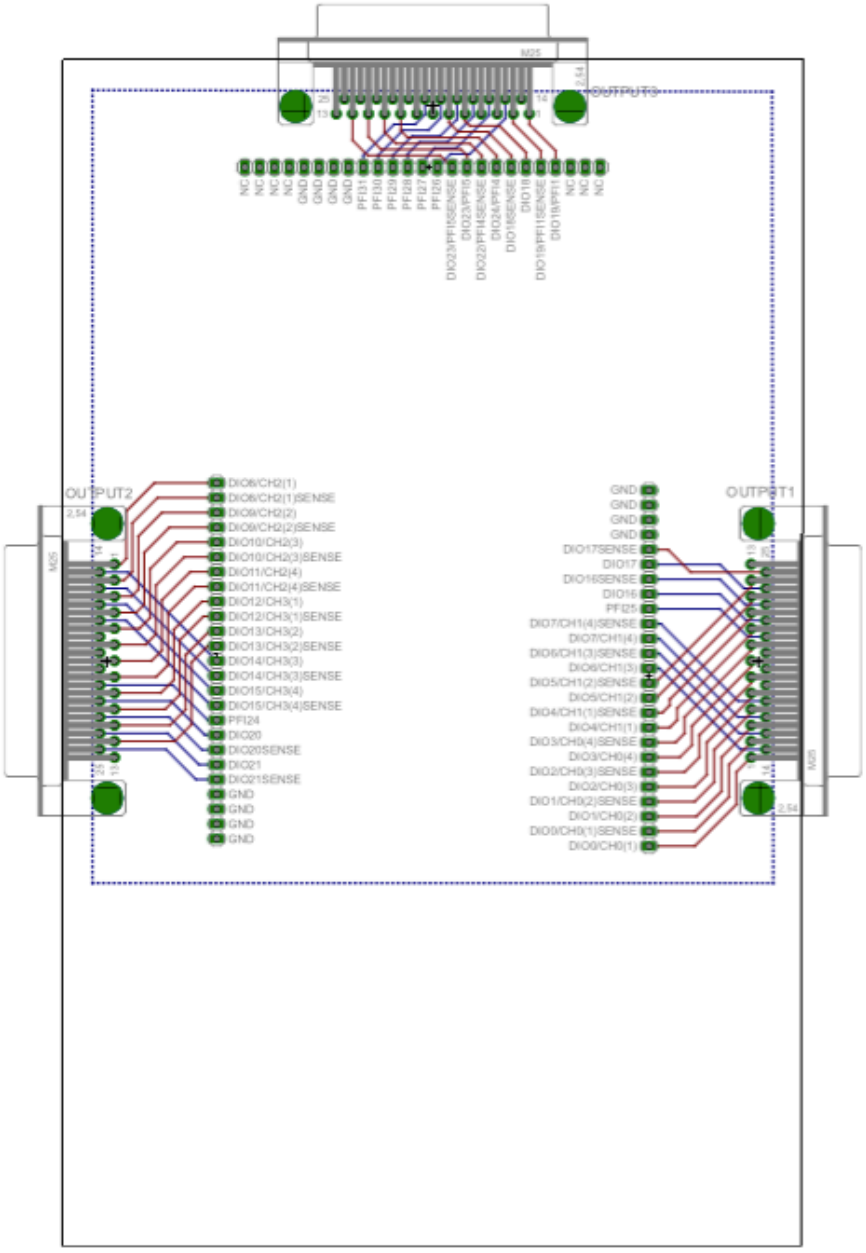


Figure 21: Breakout Board Proposed Board Layout

This design is very similar to the bench top PXI's load board setup, where all cable outputs are accessible through a single interface board. Students that are proficient on that system should have no trouble transitioning to this setup. The spacing

between connectors and headers, along with overall board size, was chosen to accommodate a standard 2.2”x7” breadboard.

4.2 Programming Demos

The LED Multisite Demo provided with the STS system is still compatible with the new load board, even though the LED structure changed somewhat between the two boards. A new switching virtual device was made, to accommodate the new relay structure, but the LabVIEW code was ultimately left unchanged, and left on the STS for students to demo multisite. The output of the Engage LED Demo is shown below.

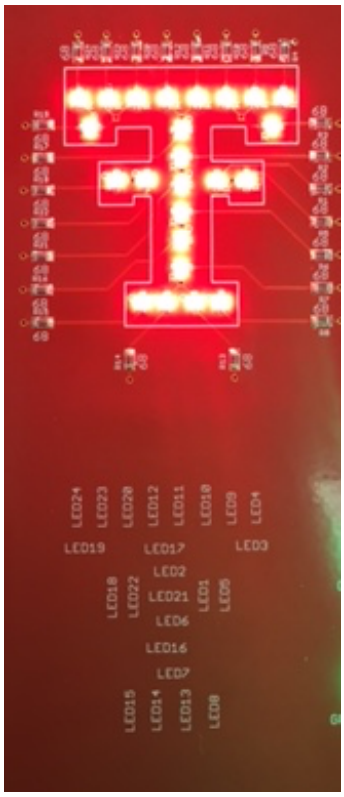


Figure 22: Engage LED Demo Output

Several undergraduate lab students began working on class demos as soon as the load board was available for testing. This project was intended to continue past the point of this thesis deadline, so instead of detailing the exact programming behind the demos, a brief overview of integrating TestStand’s Semiconductor Module with traditional testing programs will be explained.

4.2.1 Pin Map API

Semiconductor Module adds the ability for programmers to load what is called a "Pin Map" into the Test Stand sequence. It is essentially an XML code, when, given a template, can be customized to whatever device is in use. Below is a sample pin map for a logic gate in TI's "Little Logic" series.

```
- <PinMap
  xsi:schemaLocation="http://www.ni.com/TestStand/SemiconductorModule/PinMap.xsd
  C:/Program%20Files%20(x86)/National%20Instruments/TestStand%
  202012/Components/Schemas/NI_SemiconductorModule/PinMap.xsd"
  xmlns:pm="http://www.ni.com/TestStand/SemiconductorModule/PinMap.xsd"
  xmlns="http://www.ni.com/TestStand/SemiconductorModule/PinMap.xsd"
  xmlns:xsi="http://www.w3.org/2001/XMLSchema-instance" schemaVersion="1.0">
      <!-- Four site example pin map -->
    - <Instruments>
        <NIHSDIOInstrument numberOfChannels="24" name="HSDIO0"/>
      - <Instrument name="R1" instrumentTypeId="Switch">
        - <ChannelGroup id="">
            <Channel id="0"/>
          </ChannelGroup>
        </Instrument>
    </Instruments>
    - <Pins>
        <DUTPin name="A1F_B"/>
        <DUTPin name="A3F_VCC"/>
        <DUTPin name="A10F_A"/>
        <DUTPin name="A2F_Y"/>
        <DUTPin name="A12F_GND"/>
    </Pins>
    - <Sites>
        <Site siteNumber="0"/>
    </Sites>
    - <Connections>
          <!-- System Connections -->
          <!-- Site 0 -->
        <Connection siteNumber="0" channel="0" instrument="HSDIO0" pin="A1F_B"/>
        <Connection siteNumber="0" channel="4" instrument="HSDIO0" pin="A3F_VCC"/>
        <Connection siteNumber="0" channel="18" instrument="HSDIO0" pin="A10F_A"/>
        <Connection siteNumber="0" channel="2" instrument="HSDIO0" pin="A2F_Y"/>
        <Connection siteNumber="0" channel="22" instrument="HSDIO0" pin="A12F_GND"/>
    </Connections>
</PinMap>
```

Figure 23: Single Site Example Pin Map

What's most interesting to note in this pin map, is that the pin names under the different sites do not vary [22]. Where they do vary is what HSDIO or SMU channels they are connected to. It's very important to realize that, while this is a very powerful way of defining what channels are routed to what device pin, this is more for the LabVIEW side of the programming, *and it is still up to the programmer to define these connections through the load board*. Just because the pin map says that SMU Channel 0 is connected to V_{CC}, the relay driver and multiplexer must still be engaged to ensure that SMU Channel 0 is, in fact, connected to the pin.

Once the connections are defined, the next step is to develop LabVIEW test programs, much like one would ordinarily in TestStand. Semiconductor Module also comes with a LabVIEW add-on, where the flexibility of this pin map is demonstrated. A new input – "Semiconductor Module Context," seen in the screenshot below – lives within TestStand and is passed into LabVIEW to reference the site and sequence being used [23]. It is not a string or a file that can be simulated outside of TestStand, so the largest caveat to this system is that test VIs cannot be tested alone outside of the TestStand sequence.

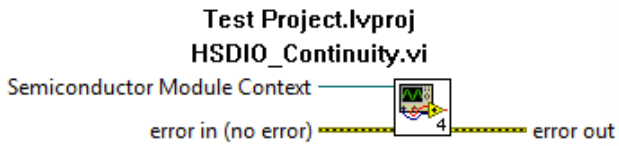


Figure 24: Example Semiconductor Module TestStand Input

Traditionally, each channel of the HSDIO must be either pre-loaded or passed into the VI from TestStand, which is not seen in the figure above. Using the Pin Map and corresponding Semiconductor Module VIs, it is possible to indicate an instrument and get the Pin Map's output, in the format accepted by the VIs that follow [22]. An example is found below.

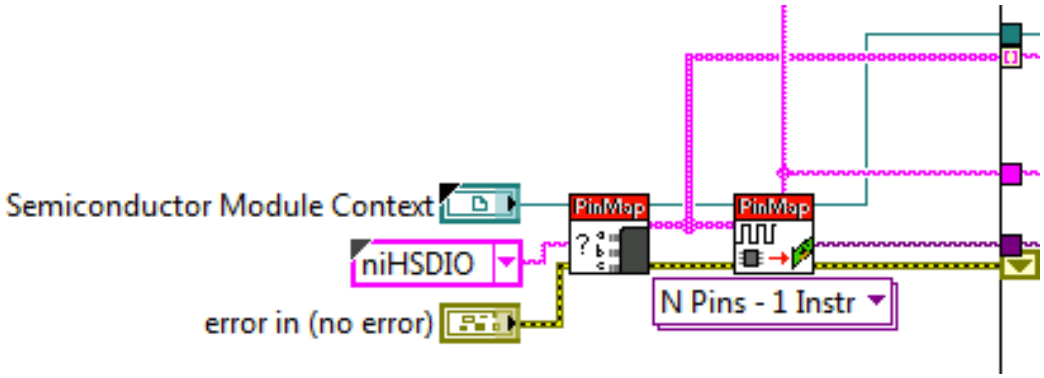


Figure 25: Use of Pin Map LabVIEW Interface

Currently, there are only several types of instrumentation that are supported by Semiconductor Module, and the two most common are the SMU (using NI DC Power driver), and the HSDIO (using NI HSDIO driver) [22]. The "Get Pin Names" VI outputs the channel list in a format accepted by either the SMU or HSDIO's driver VIs. The next Pin Map VI, "Pins to Instruments," takes those pin names and creates an output accepted

from that particular instrument. In the case of the HSDIO, one can see the Instrument Session (purple wire) and channel list (pink wire) are output to the rest of the code – all accessible without ever having to manually transfer data into the VI [23].

Initialization and Close VIs are not used in these examples, as it is customary within TestStand to include Initialize and Close VIs at the beginning and end of the entire sequence, so the device does not have to be engaged and disengaged repeatedly. Both steps are critical to still include, though, because if the device session is not closed at the end of the entire sequence, the device cannot be accessed in code again until it is reset.

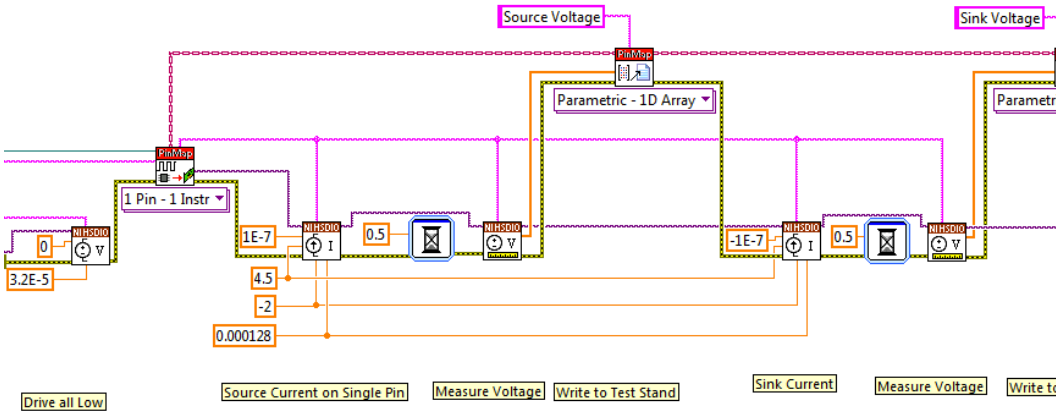
It is easy to see, in this instance, that the pin map VIs eliminate the need for hard-coding in channel names, so no code needs to be modified in the case of changing channel values. This is also how multisite is allowed – when loops are modified to allow for parallel running, and because the pin *names* are identical in the pin map, TestStand can be defined to run in however many sites are defined in the pin map. The program will open up a single, identical sequence for each site. The LabVIEW code and sequence file will be entirely the same, and the only difference between the test runs will be the channel outputs from the pin map VIs.

A demo for multisite was developed for the original STS load board, and can be found integrated into the equipment on the new load board. Verification of this software was given to the undergraduate lab students assigned to the STS. It goes much further into depth on setting up either multisite or single site tests utilizing Semiconductor Module, and is expected to be a sufficient starting point for any student interested in running test projects on the STS.

4.2.2 Pin Query Context

Another bonus from the Semiconductor Module VIs comes in the form of Pin Query Context. This eliminates the need for code within the VI to determine test pass or fail. [23] Below are images taken from LabVIEW (a) and the corresponding output now in TestStand (b).

(a)



(b)

Properties | Module | Tests | Per-Site Inputs | Options

	Test Number	Test Name	Pin	Published Data Id	Low Limit	High Limit	Scaling Factor	Base Units	Software Bin	Evaluation Type
0	101	Continuity	INPUTA_1	Source Voltage	0.02 V	1.5 V		V		Numeric Limit
1	102	Continuity	INPUTB_1	Source Voltage	0.02 V	1.5 V		V		Numeric Limit
2	103	Continuity	INPUTA_2	Source Voltage	0.02 V	1.5 V		V		Numeric Limit
3	104	Continuity	INPUTB_2	Source Voltage	0.02 V	1.5 V		V		Numeric Limit
4	105	Continuity	INPUTA_3	Source Voltage	0.02 V	1.5 V		V		Numeric Limit
5	106	Continuity	INPUTB_3	Source Voltage	0.02 V	1.5 V		V		Numeric Limit
6	107	Continuity	INPUTA_4	Source Voltage	0.02 V	1.5 V		V		Numeric Limit
7	108	Continuity	INPUTB_4	Source Voltage	0.02 V	1.5 V		V		Numeric Limit
8	109	Continuity	INPUTA_1	Sink Voltage	-1.5 V	-0.02 V		V		Numeric Limit
9	110	Continuity	INPUTB_1	Sink Voltage	-1.5 V	-0.02 V		V		Numeric Limit
10	111	Continuity	INPUTA_2	Sink Voltage	-1.5 V	-0.02 V		V		Numeric Limit
11	112	Continuity	INPUTB_2	Sink Voltage	-1.5 V	-0.02 V		V		Numeric Limit
12	113	Continuity	INPUTA_3	Sink Voltage	-1.5 V	-0.02 V		V		Numeric Limit
13	114	Continuity	INPUTB_3	Sink Voltage	-1.5 V	-0.02 V		V		Numeric Limit
14	115	Continuity	INPUTA_4	Sink Voltage	-1.5 V	-0.02 V		V		Numeric Limit
15	116	Continuity	INPUTB_4	Sink Voltage	-1.5 V	-0.02 V		V		Numeric Limit

Figure 26: PIn Query Context in (a) LabVIEW and (b) TestStand

As long as the names given in the VI match the test name (and pin) given in the test, this VI will write all of this information to the Semiconductor Test tab within TestStand, where test limits for each individual pin can be defined. Interestingly enough, this can allow for the test to be completed on all pins, but results can potentially only be logged on chosen pins [23]. For this continuity test, all pins were measured, but only results from the device's inputs contributed to whether or not the test passed or failed.

4.2.3 Device Demos and Future Work

A demo board, complete with LED indicators to all SMU and HSDIO channels, will be provided in order to demonstrate to students the connectivity within the load

board and how it relates within TestStand and LabVIEW. The original on-board LED demo will remain as a means of example for TestStand multisite setup. While demonstrating a device would give students the opportunity to see working programs, the fear was brought up for the potential to copy the LabVIEW code directly. By using a demo board, students would still need to program all tests individually, but all load board functionality will be demonstrated and, in the case of board error, tested.

A sound understanding of the system will still be required to modify the given demo code for use with other devices, which makes the two demos currently available to students sufficient for continued use. If students would like to develop their own daughter card designs, the department typically can support the funds for these simple types of projects, especially if such a board falls within the scope of Advanced Circuit's $33 student pricing.

All information from this thesis, including demo code and load board schematics, will be loaded onto an external hard drive and kept with the STS in the lab, in case a back-up is ever needed. The setup guides are held in a binder to be kept within the PSPE lab for easy student access. PDFs of what can be found in this binder can also be found on this external hard drive.

CHAPTER V

CONCLUSIONS

Currently, several undergraduate students are working to design more test demos off of the new STS load board, with the clear goal of relieving strain on the original PXI system in PSPE. As the semester draws to a close, the basic DIP20 daughter cards will be provided to interested students in each testing course, with the intent of designing their final projects off of the new load board system.

On top of that, the Advanced Modular Testing of ICs course has also been encouraging use of the new system as a means of designing final IC test projects. It is a goal in the near future to have students work interchangeably between the STS and the bench top PXI system. This provides equal working opportunities for as many students as possible. Texas Tech is one of the very first universities to implement the use of an STS, and the success of the lab's use of it so far is extremely promising.

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APPENDIX A

RELEVANT PCB IMAGES

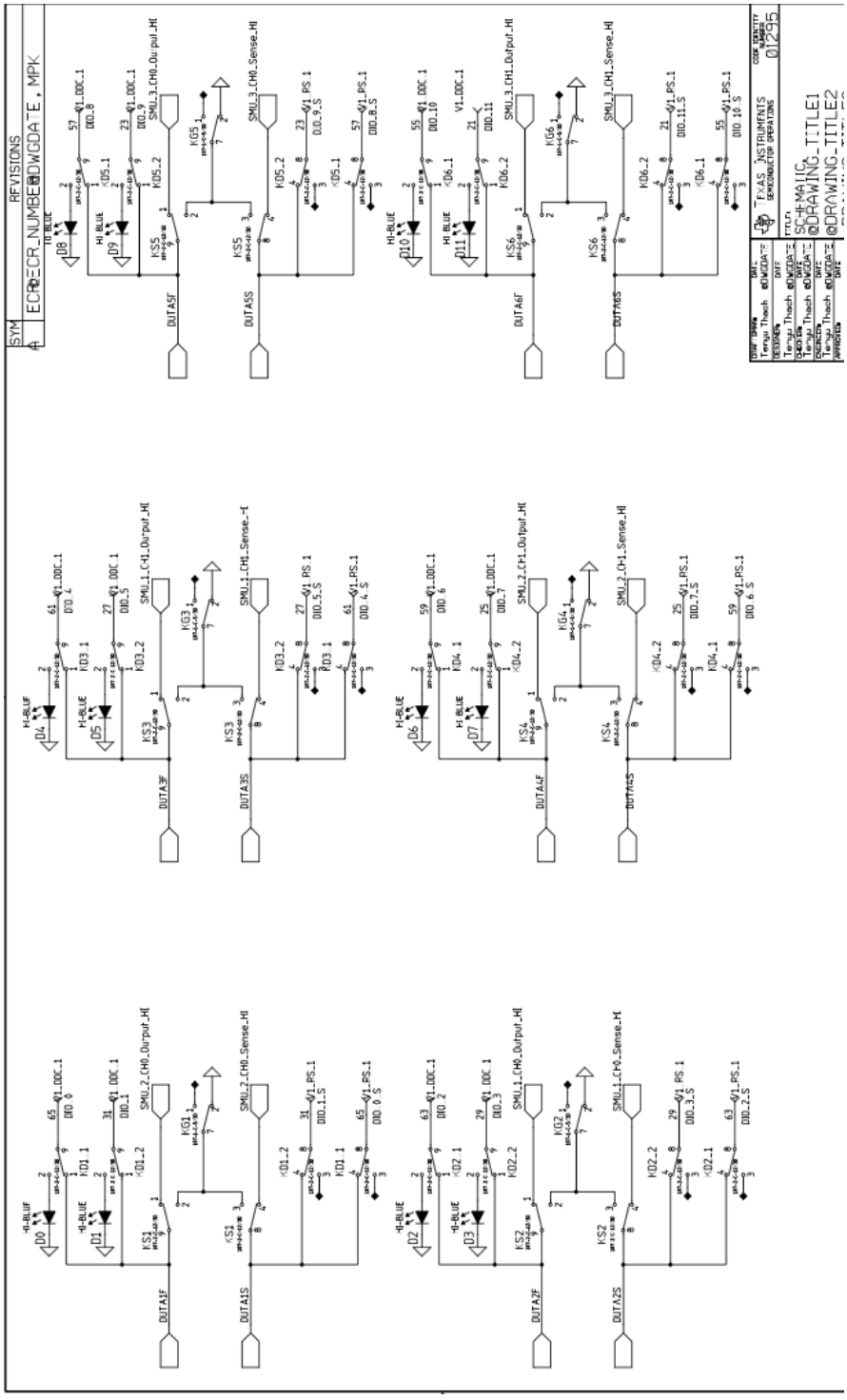

Figure 27: Donated Load Board Relay Layout Page 1

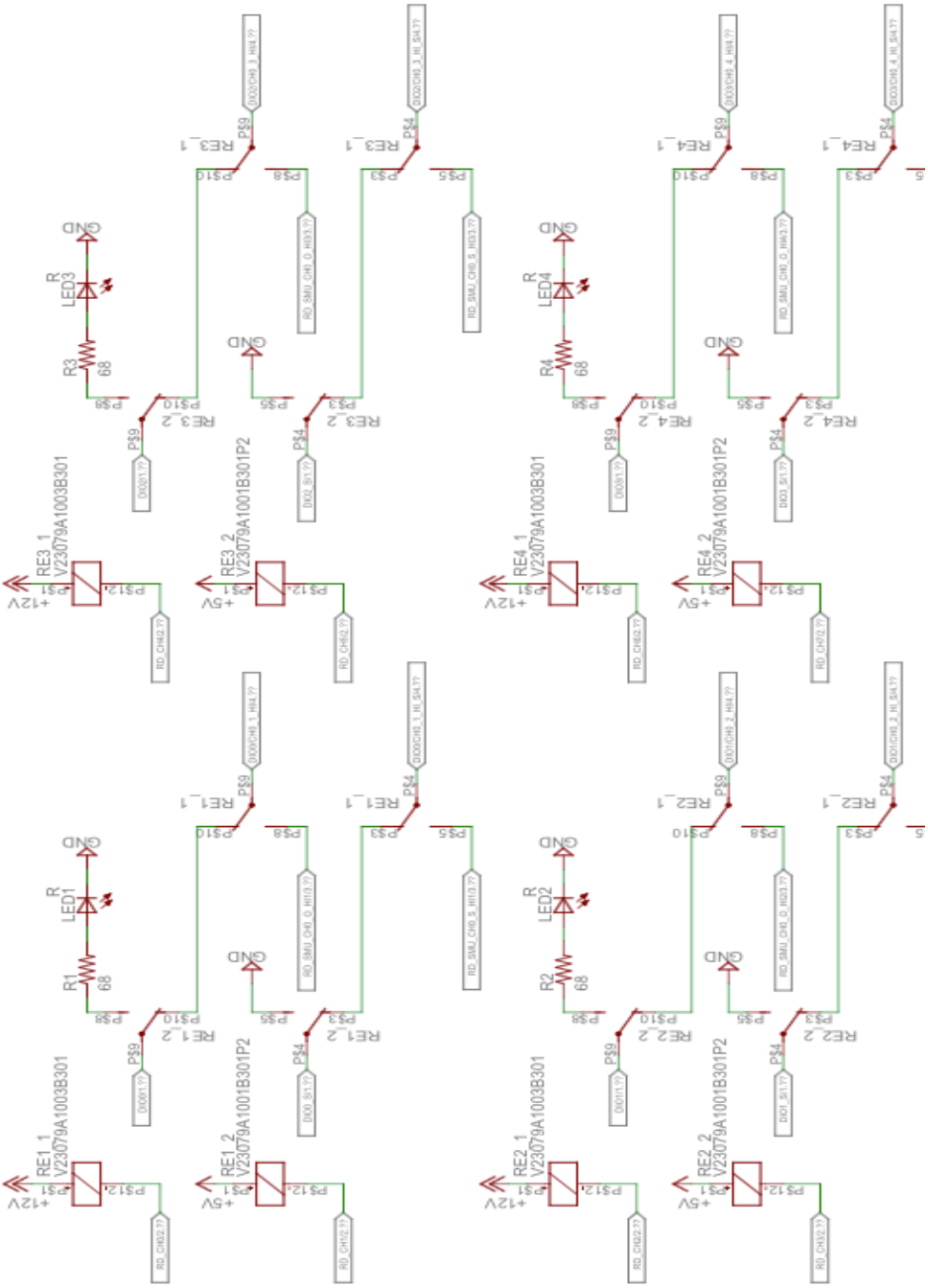

Figure 28: New Load Board Relay Layout Page 1

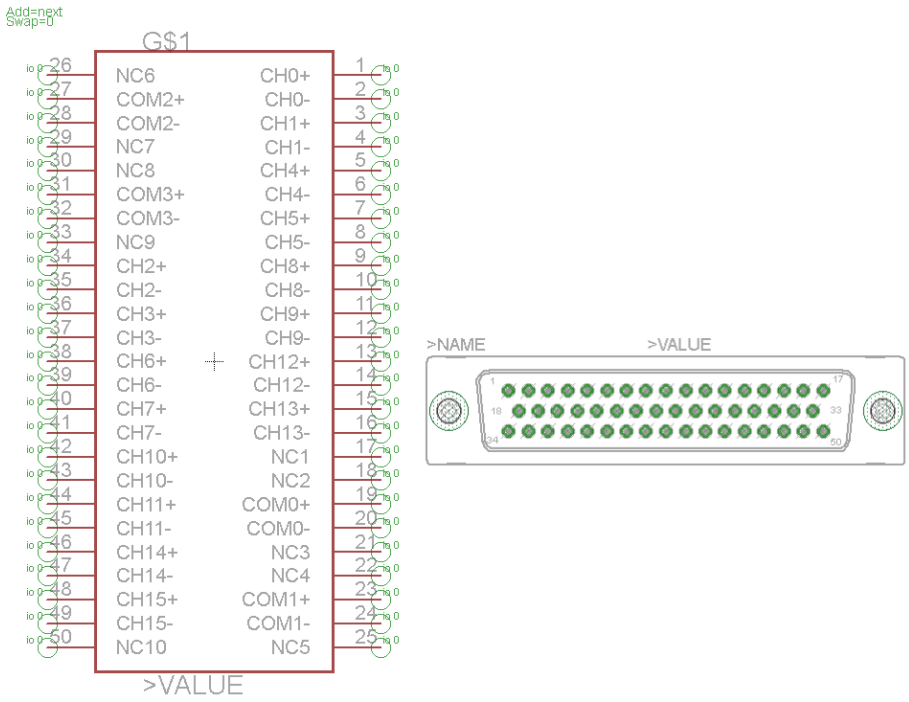

Figure 29: MUX Cable Connector 1 EagleCAD Layout

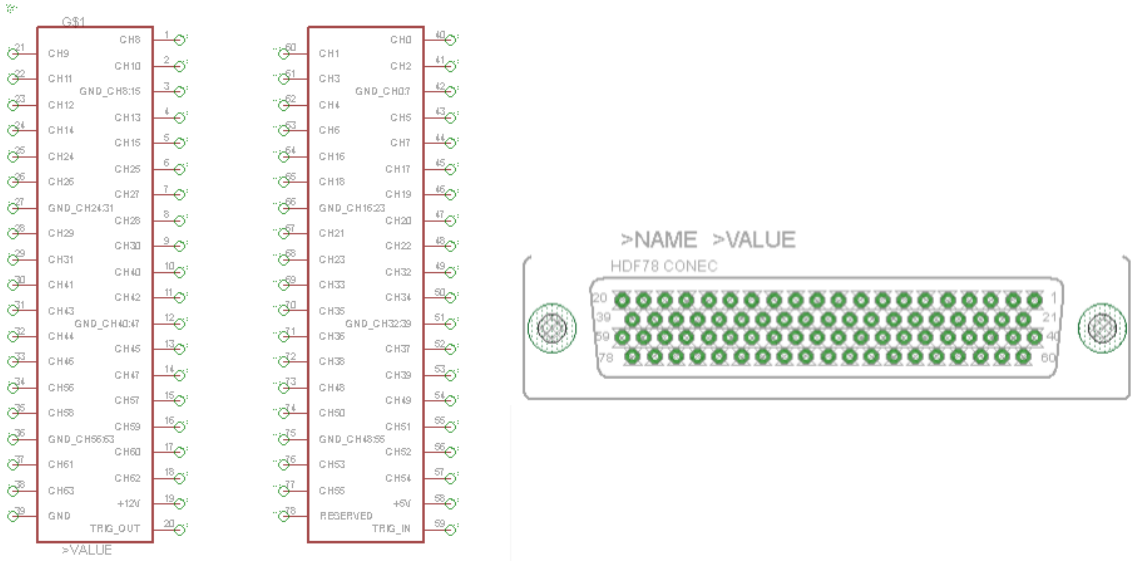

Figure 30: Relay Driver Cable EagleCAD Layout

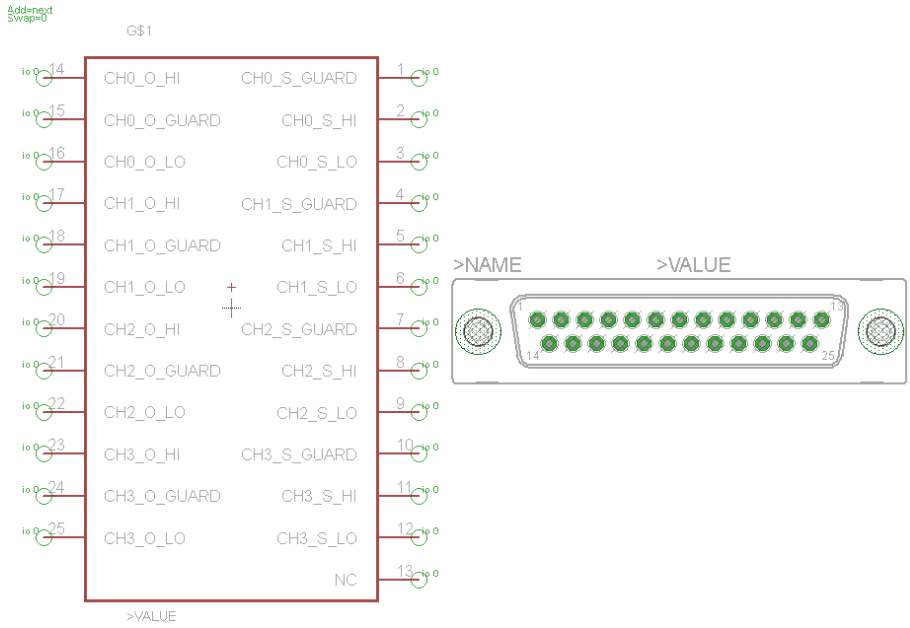

Figure 31: SMU Cable EagleCAD Layout

APPENDIX B

ROUTING SPECIFICATIONS

Table 6: SMU Trace Properties Sample

Signal	Routes	Length (mm)	Resistance (mΩ)
SMU CH0(1) OUTPUT	SMU_CH0_O_HI	63.249	103.16
	SMU_CH0_O_LO	65.832	107.38
	RD_SMU_CH0_O_HI1	56.529	92.2
	DIO0/CH0_1_HI	68.346	111.48
	TOTALS:	253.956	414.22
SMU CH0(1) SENSE	SMU_CH0_S_HI	52.641	85.86
	SMU_CH0_S_LO	52.279	85.27
	RD_SMU_CH0_S_HI1	52.367	85.41
	DIO0/CH0_1_HI_S	64.602	105.37
	TOTALS:	221.889	361.91
SMU CH0(2) OUTPUT	SMU_CH0_O_HI	63.249	103.16
	SMU_CH0_O_LO	65.832	107.38
	RD_SMU_CH0_O_HI2	61.075	99.62
	DIO1/CH0_2_HI	59.755	97.56
	TOTALS:	249.911	407.72
SMU CH0(2) SENSE	SMU_CH0_S_HI	52.641	85.86
	SMU_CH0_S_LO	52.279	85.27
	RD_SMU_CH0_S_HI2	66.185	107.95
	DIO1/CH0_2_HI_S	55.909	91.19
	TOTALS:	227.014	370.27
SMU CH0(3) OUTPUT	SMU_CH0_O_HI	63.249	103.16
	SMU_CH0_O_LO	65.832	107.38
	RD_SMU_CH0_O_HI3	90.558	147.7
	DIO2/CH0_3_HI	51.196	83.5
	TOTALS:	270.835	441.74
SMU CH0(3) SENSE	SMU_CH0_S_HI	52.641	85.86
	SMU_CH0_S_LO	52.279	85.27
	RD_SMU_CH0_S_HI3	97.227	158.58
	DIO2/CH0_3_HI_S	46.533	75.9
	TOTALS:	248.68	405.61
SMU CH0(4) OUTPUT	SMU_CH0_O_HI	63.249	103.16
	SMU_CH0_O_LO	65.832	107.38
	RD_SMU_CH0_O_HI4	101.693	165.87
	DIO3/CH0_4_HI	41.82	68.21
	TOTALS:	272.594	444.62
SMU CH0(4) SENSE	SMU_CH0_S_HI	52.641	85.86
	SMU_CH0_S_LO	52.279	85.27
	RD_SMU_CH0_S_HI4	98.585	160.8
	DIO3/CH0_4_HI_S	38.148	62.22
	TOTALS:	241.653	394.15

Table 7: HSDIO Trace Properties Sample

Signal	Routes	Length (mm)	Resistance (mΩ)
DIO0 OUTPUT	DIO0	97.564	190.96
	DIO0/CH0_1_HI	68.346	111.48
	TOTALS:	165.91	302.44
DIO0 SENSE	DIO0_S	36.733	71.9
	DIO0/CH0_1_HI_S	64.602	105.37
	TOTALS:	101.335	177.27
DIO1 OUTPUT	DIO1	82.046	160.48
	DIO1/CH0_2_HI	59.755	97.56
	TOTALS:	141.801	258.04
DIO1 SENSE	DIO1_S	39.963	78.22
	DIO1/CH0_2_HI_S	55.909	91.19
	TOTALS:	95.872	169.41
DIO2 OUTPUT	DIO2	83.146	232.48
	DIO2/CH0_3_HI	51.196	83.5
	TOTALS:	134.342	315.98
DIO2 SENSE	DIO2_S	87.473	244.58
	DIO2/CH0_3_HI_S	46.533	75.9
	TOTALS:	134.006	320.48
DIO3 OUTPUT	DIO3	57.904	113.33
	DIO3/CH0_4_HI	41.82	68.21
	TOTALS:	99.724	181.54
DIO3 SENSE	DIO3_S	62.402	122.14
	DIO3/CH0_4_HI_S	38.148	62.22
	TOTALS:	100.55	184.36
DIO4 OUTPUT	DIO4	61.867	172.99
	DIO4/CH1_1_HI	33.784	55.1
	TOTALS:	95.651	228.09
DIO4 SENSE	DIO4_S	74.312	145.45
	DIO4/CH1_1_HI_S	30.422	49.62
	TOTALS:	104.734	195.07
DIO5 OUTPUT	DIO5	36.365	71.18
	DIO5/CH1_2_HI	29.924	48.81
	TOTALS:	66.289	119.99
DIO5 SENSE	DIO5_S	84.228	164.86
	DIO5/CH1_2_HI_S	28.299	46.16
	TOTALS:	112.527	211.02